ABOUT BOCCACCIO

Boccaccio is an FMC-based board designed to provide machine vision interfaces to and from FPGA boards. All interfaces to and from the FPGA are in a single-ended parallel format to greatly simplify signal generation and processing. All external interfaces are LVDS pairs, providing high signal integrity and interfacing to standard cabling.

STANDARD INTERFACES

- Base Data-only Camera Link Transmitter
- Base Data-only Camera Link Receiver
- 2-wire LVDS serialized transmitter

CONFORMS TO MAJOR PORTIONS OF THE FPGA MEZZANINE CARD (FMC) VITA 57 STANDARD

- Compatible with I/O voltages of 1.4 to 3.3 V
- Suitable in low pin count (LPC) and high pin count (HPC) configurations and matches FMC standard card widths
CAMERA LINK RECEIVER

- SDR side launch mini Camera Link connector
- Video data only; no camera control or serial communication signals
- National Semiconductor DS90CR288A LVDS 28-bit Receiver
  - 20 MHz to 85 MHz clock support
  - Worst case power consumption < 270 mW

CAMERA LINK

- SDR side launch mini Camera Link connector
- Video data only; no camera control or serial communication signals
- National Semiconductor DS90CR287 LVDS 28-bit Transmitter
  - 20 MHz to 85 MHz clock support
  - Worst case power consumption < 250 mW

10b SERIALIZER TRANSMITTER

- Molex 501331-0607 locking vertical launch 6-pin connector
- National Semiconductor DS92LV1021A 10-bit Serializer
  - 16 MHz to 40 MHz clock support (400 Mbps)
  - Worst case power consumption < 250 mW
  - Onboard switch provides the ability to enable or disable each transceiver individually